Frontier Interdisciplinary Strategy

Research Report on Frontier Interdisciplinary Photonics-Electronics Convergence and Integration

Frontier Interdisciplinary Photonics-Electronics Convergence and Integration Research Team

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Abstract

Photonics-electronics convergence and integration (PECI) technology represents a pivotal breakthrough in addressing the limitations of computing power, communication speed, and energy consumption in the post-Moore era, holding significant strategic value. By integrating the high bandwidth and low-loss transmission of photons with the high-precision computing and storage capabilities of electrons, this technology has demonstrated substantial potential across various fields, including optical communication, defense, artificial intelligence, and intelligent perception. However, it confronts multifaceted challenges related to material compatibility, multi-dimensional tuning mechanisms of optical fields, design theories, and process platforms.

The global competition in this domain is intense. The United States, through strategic initiatives such as DARPA's "Electronics Resurgence Initiative", has taken the lead in photonic-electronic convergence innovation, with its industry, exemplified by Intel, achieving remarkable results in high-speed SerDes and satellite-to-ground laser communication. Europe has supported the development of the photonics industry through the Horizon program, while Japan has made long-term investments in PECI system technology, with NTT realizing a 1.2Tb/s coherent optical module. The global process platform is characterized by a three-tier structure, comprising university research platforms, national research and development centers, and leading enterprise-built platforms.

China, although a latecomer in this field, has experienced rapid development and has reached international advanced levels in some areas. The National Information Optoelectronics Innovation Center has achieved industrialization of 100G-400G silicon photonics transceiver chips. Tsinghua University has developed the photonic-electronic convergence chip ACCEL, which has significantly improved energy efficiency. The 504th China Academy of space technology has realized 10Gbps satellite-to-ground laser communication. However, China still faces challenges such as a fragmented process platform, processing capabilities lagging behind international leading levels, a lack of

core design software, insufficient packaging standards and large-scale manufacturing capabilities, and the need to strengthen system-level applications.

In light of the above, this report proposes the following development suggestions: at the chip level, focus on breaking through silicon-based mid-infrared photonic-electronic integration, ultra-large-scale heterogeneous photonic-electronic integration chips, multi-functional and multi-channel reconfigurable microwave photonic chips, and photonic intelligent chips. At the system and application level, deploy integrated sensing and computing technology for high-precision multi-dimensional perception imaging, spatial laser backbone communication networking technology, ultra-large capacity and ultra-low power optical communication chips and modules, multi-chiplet optical computing/sensing system, co-packaged integration and high-speed chip-to-chip optical I/O technology, and unified process platform technology for PECI. At the policy and mechanism level, it is recommended to launch the " Major Research Plan for Photonics-Electronics Convergence and Integration " under the National Natural Science Foundation of China to strengthen systematic research on PECI, increase R&D investment in core processes, improve the industrial ecosystem, establish a standardization system, and promote integrated and coordinated development.

PECI technology is a strategic high ground in future information technology competition. There is an urgent need for top-level design and resource integration at the national level to break through the entire chain, build an independent and controllable innovation ecosystem, achieve integrated breakthroughs in "light-electricity-computation" and support comprehensive advancements in China's information technology field.

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Ⅰ. Strategic Position

Microelectronics and optoelectronics are crucial foundations and core technological lifelines for the development of modern information technology. Over the past 50 years, the integration scale of microelectronic devices represented by transistors has increased by 50 million times, driving the miniaturization and intelligence of electronic equipment, greatly improving computing power, reducing power consumption, and supporting the new generation of artificial intelligence revolution. Integrated optoelectronic devices represented by semiconductor lasers have propelled the rapid development of modern communication and network technologies, facilitating the large-scale growth of the internet industry.

Photons and electrons are the two most important information carriers, each with distinct physical characteristics that confer unique advantages in information systems. Microelectronics technology boasts high spectral resolution, supporting rapid storage, writing, and reading of large amounts of data, making it suitable for high-speed digital computing and information processing. With transistors as the basic unit, integration and performance can be enhanced through the reduction of process dimensions at different nodes. However, as two-dimensional transistor structures approach physical limits and manufacturing costs rise significantly, the performance of individual chips encounters bottlenecks. Communication rates and power consumption between chips become major constraints on system performance. Optoelectronics, on the other hand, operates at frequencies typically two orders of magnitude higher than microelectronics, offering excellent bandwidth performance. Additionally, multi-physical dimension control of photons can further significantly increase the transmission rate of optoelectronic information. Photons are typically transmitted through low-loss waveguide structures, resulting in low transmission loss and suitability for long-distance transmission of high-capacity information. However, the basic units of optoelectronic devices are diverse, and due to the diffraction limit, they cannot achieve scaled-down size reduction. The current level of integration is comparable to that of

microelectronics in the 1980s.

The integration of optoelectronics and microelectronics has the potential to achieve organic fusion, addressing bottlenecks in speed, energy consumption, and computing power in the post-Moore era, while fostering the emergence of new intelligent applications.

(1) In optical communication and interconnection, the rapid growth in demand for data communication capacity poses more stringent challenges to the speed and bandwidth of related devices. High-speed, high-capacity optoelectronic devices are particularly critical in addressing this issue. Microelectronics integration technology, with its early start, has hit the bottleneck of Moore's Law. The integration of optoelectronics and microelectronics technology promises to array and tightly integrate functional components such as high-speed modulation, high-speed reception, and multi-dimensional multiplexing required for optical interconnection systems. This can significantly reduce the size of optoelectronic integrated chips and modules, facilitating expansion and continuous performance upgrades, energy consumption reduction, and cost reduction.

(2) In radar applications, the integration of optoelectronics and microelectronics technology enables the full integration of radio frequency front ends, digital chips, and optical processing chips, achieving digital-analog integration and optical-electrical integration. This leads to low-cost, large-scale production of radar systems and high-density, low-power, high-speed information processing.

(3) In photonic artificial intelligence acceleration computing, deep learning with artificial neural networks is a key technology. Its neural network algorithms involve numerous multiplication and accumulation calculations. Traditional central processors based on electrical networks struggle to perform these operations, especially when handling large-scale parallel signal processing. Central processors based on the von Neumann architecture encounter technical bottlenecks, limiting computational efficiency, accuracy, and precision. Furthermore, the energy consumption of electrical interconnects is enormous, and their speed and bandwidth cannot meet the explosive

growth of artificial intelligence. Optoelectronic integrated computing chips can significantly accelerate specific computing methods such as artificial intelligence deep neural networks and neuromorphic computing, addressing the contradiction between rapidly growing computing demand and the failure of Moore's Law in electronic chips. They offer high bandwidth, high parallel processing, low latency, and low power consumption, providing a new path to solve the computing power challenges of artificial intelligence.

(4) In intelligent optical sensing, the further integration of optoelectronics and microelectronics effectively reduces the number of discrete components within sensors, achieving optoelectronic synergy for lower power consumption and flexible reconfigurability. Additionally, the integration technology of optoelectronics and microelectronics enables chip-level integration of back-end devices such as optical interconnection transmission and monolithic integrated digital circuit preprocessing circuits. This leads to the miniaturization of optical sensors, significantly improving their stability, environmental adaptability, and expanding their application scenarios to fully meet the technical requirements of the internet of everything era.

Considering the demands of national economic development and defense military construction, photonics-electronics convergence and integration (PECI) technology holds significant application value in China. This direction provides a new opportunity for the development of China's optoelectronics field and is an essential path for large-scale practical applications.

II. Development Patterns and Research Characteristics

1. Main Scientific and Technical Issues

The development of PECI requires the multifaceted integration of materials, design, processes, chips, packaging, and system applications across the entire chain. Specifically, the facing scientific and technical challenges are as follows:

(1) Collaborative Design Theories and Methods for PECI

In the aspect of co-design for PECI, it is necessary to gradually improve the basic theory of PECI, establish an integrated environment for PECI design, and develop specialized tools for the entire design process, including physical simulation, device modeling, link simulation, layout design, and verification, to form new design methodologies. Meanwhile, it is essential to develop an PECI component library tailored for design automation, leveraging domestic process platforms, and establish an autonomous and controllable integrated optoelectronic design ecosystem.

(2) Heterogeneous Integration Methods for Multi-Material Systems

Currently, the primary material integration platforms for optoelectronics include III-V compounds, silicon-based, silicon nitride, and lithium niobate. Among them, the III-V platform can achieve full integration of all functions from light emission, transmission to detection, but it suffers from high wafer costs, limited sizes, and difficulty in integrating with silicon-based microelectronic chips. The silicon-based platform, with mature fabrication processes, compact structures, and compatibility with microelectronic CMOS processes, is an ideal platform for integration with microelectronics. However, as an indirect bandgap material, it faces challenges in achieving efficient light emission, making silicon-based on-chip light sources one of the major bottlenecks limiting its development. The silicon nitride platform, known for its low loss and high-power handling capabilities, is a significant platform for passive

devices but struggles with achieving high-speed modulation functions. The thin-film lithium niobate platform, characterized by excellent electro-optic modulation and other optical and acoustic properties, along with low transmission losses, represents a new generation of integrated optical platforms. Nonetheless, its larger device size poses challenges for integration with silicon-based microelectronic chips. Due to the distinct characteristics and advantages of the current integrated material systems, achieving high-performance PECI devices through a single material system remains challenging. The key technology and limiting factor in this regard is how to achieve multi-material system integration and device performance improvement through hybrid integration approaches.

(3) Multi-Dimensional Tuning Mechanisms for PECI

Photons and electrons possess multiple physical parameters such as amplitude, polarization, frequency, temporal distribution, spatial distribution, phase, and spin. Wavelength division multiplexing and polarization multiplexing technologies have significantly enhanced the transmission rates of optical communications. In recent years, on-chip mode multiplexing and spatial multiplexing technologies have emerged as research hotspots, further expanding the utilization of physical resources. The key technologies and limiting factors in this area involve efficiently expanding the modulation dimensions of physical parameters to enhance system capacity, particularly regarding on-chip multi-dimensional integration involving spatial modes and their compatibility with optical fibers, optimizing core system performance such as inter-channel crosstalk and system insertion loss, and improving the processing capabilities of multi-dimensional modulation devices. Achieving breakthroughs in these areas requires advancements in material systems, device design, processing platforms, and intelligent control.

(4) Multi-Functional and Efficient Integration Technologies

As the demand for sensing, storage, processing, and communication increases in

new-generation information systems, it becomes necessary to integrate different functional structures, devices, and chips into a unified system. Smart microsystem technology, which considers optoelectronic and microelectronic chips as the core hardware organized according to specific architectures and supplemented by intelligent algorithms, represents a significant technological route beyond Moore's Law and a disruptive technology for the next generation of information technology. The key technologies and limiting factors in this regard involve collaborative design for functional units such as sensing, storage, computing, energy, and actuation, as well as heterogeneous integration processes across different modules.

(5) Efficient Interaction Mechanisms in Multi-Physics Environments

The integration of optoelectronics and microelectronics has gradually evolved from traditional packaging integration based on discrete chips to advanced co-packaging integration on single substrates with multiple chiplets, and further towards three-dimensional hybrid integration on single substrates. This evolution has led to increased interconnect density and speed while reducing interconnect power consumption. Currently, through hybrid bonding technology, co-packaging integration has achieved an interconnect density of 10μm pitch and is expected to further reduce to 5μm. However, the parasitic capacitance associated with packaging and the corresponding electrostatic discharge structures limit further reductions in power consumption. CMOS-compatible single-substrate integration offers the best performance in terms of speed and power consumption but requires the development of corresponding processes. Additionally, the overall manufacturing costs are high due to the significantly larger size of optoelectronic devices compared to microelectronic devices. The key technologies and limiting factors in this area involve achieving breakthroughs in design, processing, and packaging technologies for the integration of optoelectronics and microelectronics.

2. Future Trends

The future of chip technology is rapidly moving towards the integration of optoelectronics and microelectronics, aiming to achieve complementary advantages between the two and overcome bottlenecks in high-speed, low-power, and intelligent information technology. Addressing future application scenarios requires urgent solutions to key issues such as the theoretical framework of PECI, collaborative design theories and methods for PECI, advanced processes and materials for PECI, and manufacturing, packaging, and testing technologies for PECI chips.

(1) High-Density Silicon-Based PECI Chip

Silicon-based PECI technology focuses on researching and developing large-scale integrated chips that use optoelectronics as the information carrier on a silicon platform. This technology relies on silicon or compatible materials and employs CMOS processes to simultaneously fabricate photonic and electronic functional devices on a silicon substrate, resulting in large-scale integrated chips that integrate both photonic and electronic functionalities. Silicon-based PECI technology leverages the maturity and cost-effectiveness of microelectronic processes while harnessing the unique characteristics of photonic devices and systems, such as extremely high bandwidth, ultra-fast transmission rates, and high interference immunity.

(2) Ultra-Large-Scale Chip Integration

Ultra-large-scale integration technology for optoelectronic fusion involves the heterogeneous integration of multiple material systems, such as InP, silicon-based, and lithium niobate materials, to achieve large-scale, array-based, and multi-functional photonic device integration. This includes devices such as lasers, modulators, amplifiers, detectors, polarization controllers, couplers, and filters. Currently, three main trends are emerging: wafer-level PECI achieved through the three-dimensional integration of photonic integrated wafers and integrated circuit wafers; optoelectronic hybrid integration of silicon-based photonic integrated circuits and silicon-based microelectronic integrated circuits on the same wafer; and PECI based on the

heterogeneous compatibility of multiple materials.

(3) Multi-Functional, Multi-Channel, and Reconfigurable Microwave Photonic Integrated Chips

As a system-level application of PECI chips, microwave photonic chips combine the advantages of microwave technology and photonic technology to generate, process, transmit, and receive high-frequency broadband microwave signals in the optical domain. Microwave photonic technology fully leverages the benefits of broadband and low-loss transmission in optical fibers, offering features such as large bandwidth, low transmission loss, lightweight, rapid reconfigurability, and immunity to electromagnetic interference. It has become a trending solution and effective approach for future information processing and access. Compared to discrete systems, microwave photonic chips significantly reduce system volume and power consumption, eliminate the cost of individually packaging each device, and minimize coupling losses between devices, thereby enhancing system stability. Future optimization directions for multi-functional, multi-channel, and reconfigurable microwave photonic chips include microwave photonic passive core devices, microwave photonic active core devices, and microwave photonic array devices. The aim is to achieve ultra-high integration and stability through a single chip system.

(4) Photonic Intelligent Chips

PECI computing chips can achieve specific computing methods such as deep neural networks and large-scale tensor computations in artificial intelligence, significantly accelerating traditional electronic chip computing and addressing the contradiction between rapidly growing computing demand and the diminishing returns of Moore's Law. These chips are characterized by high bandwidth, multi-dimensional parallel processing, low latency, and low power consumption. The integration of photonic technology and artificial intelligence technology aims to develop intelligent

photonic processors and photonic accelerator chips, which are currently research frontiers and focal points globally. Photonic intelligent chips integrate the advantages of brain-inspired computing, optical computing, and optical interconnectivity, significantly enhancing the speed and energy efficiency of intelligent computing. However, photonic brain-inspired computing is still in its early research stages. Currently available artificial intelligence-based microwave photonic systems have demonstrated applications in areas such as photonic analog-to-digital conversion, instantaneous spectrum measurement, and integrated optical neural networks, offering improved computing capabilities with high energy efficiency. By combining the broadband capabilities, flexibility, and high-speed processing of microwave photonics with artificial intelligence algorithms for signal distortion correction and compensation, mismatch and noise suppression, and intelligent learning and decision-making, signal system optimization and autonomous learning can be achieved.

Ⅲ. Domestic and International Development Status

1. International Strategic Layout in PECI Technology

Recognizing the enormous potential and advantages of PECI, major developed and developing countries have made plans and layouts in this field. In the US, DARPA initiated the Diverse Available Heterogeneous Integration (DAHI) program in 2011, deploying the Microelectronics and Photonic Heterogeneous Integration (E-PHI) project. This led to the introduction of the 90WG and 45CLO optoelectronic monolithic integration process platforms. Recently, under the Electronics Resurgence Initiative (ERI), projects like LUMOS for silicon-based light source integration in microscale optical systems, PIPES for ultra-scalable optical interconnects, and POEM for efficient inter-chip and on-chip communication have been launched, promoting multi-material systems and multi-functional PECI. Departments like the US Department of Energy have also introduced projects targeting multi-board interconnects in high-performance computing systems.

In Europe, under the Horizon program, the 21st-century Photonics Research Initiative has been launched to promote the development of the optoelectronic industry, funding projects such as high-speed Ge/Si modulation detection, CMOS-compatible SiN platforms, and new material system integration for silicon nitride platforms.

Japan has been conducting research on the basic technology development of PECI systems since 2010, aiming to solve the high-speed data communication bottleneck between large-scale integrated circuit chips and achieve efficient inter-chip and on-chip interconnects for computing systems.

2. International Development Status of Process Technology

PECI devices and chips involve various material systems such as silicon, SiN, and lithium niobate, encompassing both passive and active devices. Facing the large-scale development of future integration, both high-performance passive and active devices

are crucial. Notably, large-scale integrated chips have stringent uniformity requirements for passive devices, posing urgent demands for high-level processing capabilities. This signifies that the importance of process technology capabilities in the development of PECI has entered an unprecedented new phase.

Globally, the development of optoelectronic chip processing platforms can be divided into three levels. The first level comprises university research institutes represented by Singapore's AMF and the Netherlands' Tu/e. For instance, AMF, affiliated with the Agency for Science, Technology and Research (A*STAR) in Singapore, focuses on silicon-based optoelectronic technology and advanced MEMS technology. It boasts a 45nm CMOS pilot line for 12-inch wafers using immersion lithography and an 180nm advanced process line for 8-inch wafers. Tu/e has established an InP-based integrated optoelectronic chip platform, currently the only unit internationally offering InP-based MPW foundry services.

The second level consists of government-led non-profit innovation centers represented by Belgium's IMEC. IMEC has over 10,000 square meters of cleanrooms, equipped with EUV lithography and a 12-inch CMOS pilot line, as well as an 8-inch advanced technology R&D line, making it a European hub for microelectronics technology innovation. In 2015, the US established AIM Photonics, led by the State University of New York, with a total investment of $600 million to support the development of future nanotechnology by large enterprises and startups.

The third level comprises platforms built by integrated electronics companies, most of which have deep expertise in CMOS, such as Intel and GlobalFoundries. Notably, GlobalFoundries has introduced a 45-nm CMOS fully compatible silicon photonic chip foundry platform, representing the highest process node currently used in the industry for manufacturing optoelectronic chips.

3. Development Status of PECI in the Communication Field

In the communication field, PECI technology mainly addresses high-speed, low-latency optoelectronic interconnects between sensing, computing, and sensing nodes

within platforms. It also facilitates high-speed, reliable, and anti-interference multi-mode information transmission between platforms such as vehicles, ships, aircraft, and satellites. This technology meets the demands of signal transmission, reception, and processing, aiming to significantly reduce the size, weight, and energy consumption of payloads. Specifically, the transmitting end comprises lasers, modulators, and supporting drive circuits for high-speed electro-optic signal conversion. The receiving end includes detectors and TIA circuits for optoelectronic conversion and electrical signal amplification. Signal processing involves multi-dimensional multiplexers, high-performance optical switches, wavelength polarization control units, and high-bandwidth digital-to-analog/analog-to-digital converters for channel multiplexing, routing, key performance regulation, and information type conversion of optoelectronic signals.

In short-distance optical interconnects, companies like Lockheed Martin and Ayar Labs have conducted research on multi-node fusion sensing and computing multi-system integration platforms in 2022. These platforms utilize high-bandwidth, low-latency optical interconnect buses to create a high-performance "fusion aperture" combat system. They achieve an interconnect bandwidth of 11.2 Tb/s through the optical bus, reducing the overall platform power consumption to one-fifth of the current level and decreasing the payload size by an order of magnitude.

In terms of basic devices, Intel integrated a 6-bit 112GS/s ADC into its 224Gb/s SerDes in 2022, achieving an effective number of bits of 4.5. In satellite-to-satellite/satellite-to-ground communications, the US completed the TB-level Infrared Transmission project (TBIRD) in 2022. This project utilized PECI technology to demonstrate a 100Gb/s satellite-to-ground downlink laser communication test with a payload weight of only 2.24kg, achieving the highest in-orbit laser communication rate and lightest payload mass ever recorded.

In cross-domain communications spanning air, ground, and sea, Google's subsidiary Aalyria utilized highly integrated coherent optical communication modules in its TightBeam project in September 2022. This achieved ultra-high-speed coherent

optical communication of 1.6 Tb/s between stratospheric balloons, with a communication payload weight controlled within 10kg. In unmanned platform communications, General Atomics utilized ultra-lightweight, low-power laser communication terminals in October 2022 to demonstrate anti-jamming, low probability of intercept/low probability of detection (LPI/LPD) laser communication between two drones. The terminal weighed only 3.5kg and consumed less than 20W of power.

In underwater/cross-media optical communications, Sonardyne introduced an ultra-small wireless optical communication device for underwater AUVs, ROVs, and other unmanned underwater vehicles. This device achieved a communication distance of 150m and a communication rate of 10Mb/s.

The European Union has also made significant progress in PECI for communication applications. In 2016, they launched the silicon-based Monolithic OptoElectronic Devices (MODES) project to research passive and active photonic devices based on III-V materials and silicon waveguides for short-distance optical interconnects. In satellite-to-satellite/satellite-to-ground communications, they initiated the EDRS project in 2016, employing highly integrated coherent communication modules to realize two high-orbit satellites, EDRS-A and EDRS-C, with a communication rate of 2.8Gb/s and a communication distance of 45,000-75,000km. Additionally, in 2020, they collaborated with the US on the ALCOS project, utilizing lightweight, multi-spectral laser communication equipment mounted on MQ-9 Reaper drones to achieve the world's first drone-to-satellite multi-spectral laser communication with a rate of 1.8Gb/s and a distance of 40,000km.

Japan has also been active in this field, initiating the second phase of the Photonics Electronics Convergence Systems Technology (PECST-II) project in 2012. By 2022, they aimed to achieve an PECI interconnect module with a total bandwidth of 10 Tb/s and an energy efficiency of 1mW/Gb/s. In 2022, they announced an ultra-small optical transceiver engine with a single-chip bandwidth of 400Gb/s, targeted at compact AI computing applications. NTT achieved a 1.2Tb/s total bandwidth coherent optical

communication module through co-packaged heterogeneous integration in 2022, with the driver chip achieving a bandwidth of over 65GHz using CMOS technology.

Overall, the development trends in PECI technology for communication applications include ultra-high speeds (with typical communication rates increasing from Mb/s to Gb/s or even Tb/s), multi-platform and networked capabilities (featuring laser communication links between satellites, high-altitude reconnaissance aircraft, drones, ships, and other platforms), multi-spectral integration (combining UV, visible light, infrared wide-spectrum communication with laser/microwave radio frequency fusion), and multi-functional integration (combining laser communication with laser ranging and optical imaging for sensing, transmission, and computing).

4. Development Status of PECI in the Field of National Defense

In the future society, individuals aspire to achieve a state of omniscience, omnipotence, and wisdom. For nations, the goal is to realize global real-time high-precision reconnaissance, smooth and high-speed information transmission and processing, and intelligent and accurate central decision-making. To achieve these states, China's information system needs multi-dimensional information detection capabilities covering air, space, ground, and sea, transmission and processing capabilities for massive amounts of information, and ultra-low power consumption payload integration capabilities. However, based on traditional microwave and electronic technologies, limited by bandwidth and electronic bottlenecks, it is difficult to meet the development needs of high-precision detection, fast response processing, and intelligent decision-making in the future information society.

To continue advancing significant improvements in the performance of electronic devices without relying on Moore's Law and maintain the United States' leading position, the Defense Advanced Research Projects Agency (DARPA) launched the "Electronics Resurgence Initiative" (ERI) in June 2017, which is hailed by the industry

as the next electronic revolution. DARPA's "Electronics Resurgence Initiative" is a five-year, $1.5 billion research program that involves a series of forward-looking collaboration projects between the commercial sector, defense industry, university researchers, and the Department of Defense. It requires innovative new approaches to materials, designs, and architectures for microsystems.

5. Development Status of PECI in the Field of Computing

The application of optoelectronic integrated integration in the field of computing mainly focuses on two aspects: optoelectronic hybrid interconnection and optoelectronic collaborative computing.

The driving force for the demand of optoelectronic hybrid interconnection lies in the explosive growth of network transmission bandwidth capacity in capability-based and capacity-based computing systems, with transmission rates rapidly evolving from 10Gbps to 112Gbps or even 224Gbps. Traditional electrical interconnection is limited by physical characteristics, resulting in rapid deterioration of loss and drastic reduction in drive distance at higher speeds, making it unable to meet the needs of system interconnection. Optical communication has become the main carrier of interconnection communication, replacing metal cables or printed lines from cabinet to board, and then within the board. The sinking of optical interconnection is mainly manifested in the gradual transition of optoelectronic conversion from board edge to on-board, evolving from near-package optics (NPO) to co-package optics (CPO). Currently, the chip foundation for optoelectronic hybrid integration, including PECI on a single chip, is mature at the device level, and prototype systems have been demonstrated. However, optically integrated circuits (IOs) still face challenges in meeting high reliability and convenience requirements in terms of physical form and packaging. They are also limited by heat dissipation and temperature control (as large-scale integrated circuits typically have high power consumption), and optically co-packaged devices have not yet gained widespread acceptance from system integrators

in terms of thermal reliability. Large-scale adoption awaits breakthroughs in the design of optical IO packaging, the thermal stability of packaging fixation, and the temperature stability of optical device performance. Considering flexibility and reliability, the development of optical engines in the next five years is expected to focus primarily on NPO as the main application carrier.

In the aspect of optoelectronic collaborative computing, with the rapid development of technologies such as silicon-based PECI and quantum information, optical computing technology is expected to become one of the feasible paths to meet the urgent demands of high computing power and low energy consumption in artificial intelligence. Compared with traditional electronic computing technology, optical computing technology has advantages such as high speed, high bandwidth, low power consumption, and high parallelism. Significant progress has also been made in on-chip integration. However, optical computing is still not mature enough and has only found limited applications in certain specific fields. General-purpose optical computing has not yet developed into a mature practical technology. Optical computing faces practical challenges such as high data sourcing overhead. Due to the physical characteristics of photons, it is difficult to achieve storage using light alone. Data will still need to be stored in electronic storage devices for an extended period. To perform optical computing, data must first be converted from electronic devices into optical signals, and then the output results must be converted back into electronic signals for long-term storage. The additional power consumption generated by this electro-optical/optoelectronic conversion of data is relatively high. Therefore, the current applications of optical computing are mainly concentrated in machine vision, where the input data is originally an optical signal, and in sensor systems where the signal needs to be converted into an optical signal for long-distance transmission. From another perspective, the principles of optical operations can also be interpreted as a form of computing, acting as a preprocessing stage or co-processing unit that works alongside electronic platforms for processing data records. Based on this interpretation, optical components can be leveraged to perform as much work as possible, breaking through

the bottleneck of optical-electrical data interaction at the protocol level, and utilizing the physical characteristics of optical computing and optoelectronic collaborative computing to optimize the overall computing system's latency and power consumption requirements.

Optical Neural Networks (ONNs) and photonic circuits represent a paradigm shift for AI accelerator applications and other machine learning applications. Inference tasks, particularly those for visual computing applications, can be effectively implemented using fully optical or optical-electrical hybrid systems. In the field of artificial intelligence, convolutions, Fourier transforms, random projections, and many other operations are the fundamental building blocks of deep neural network (DNN) architectures and drive most modern visual computing algorithms. These operations can also be byproducts of light-matter interactions or light propagation and can be performed nearly "for free" by linear optical components. Currently, with significant advances in on-chip photonic integration technology, ONNs are evolving from spatial optical computing to photonic chips to achieve miniaturization and chip-scale integration to meet the demands of optoelectronic collaborative computing. In 2017, researchers at the Massachusetts Institute of Technology (MIT) constructed an all-optical convolutional architecture based on a silicon-based Mach-Zehnder interferometer (MZI) optical switch array, enabling speech recognition through deep learning programming on a nanophotonic chip. The chip, composed of 56 programmable MZIs and 213 phase-shifting units cascaded together, was designed with a 1×4 neural network structure integrated onto a millimeter-scale silicon-based chip. The MZI optical switches achieve full optical interconnectivity within the plane, and the splitting ratio of the MZI optical switches can be adjusted by varying the voltage, allowing for a programmable weight matrix to be loaded onto the chip. In 2019, researchers at the University of Münster proposed an all-optical neural network chip based on a phase-change material combined with cascaded microring structures, capable of simple English letter recognition.

"Brain-like" computing is another important development direction of optical

computing. The human brain, consisting of billions of highly interconnected neurons, possesses tremendous processing capabilities. Experiments have shown that the amount of processing computed by the biological brain in one second would take a supercomputer 40 minutes to complete. Brain-like photonic chips simulate human brain computing by carrying information through photons and processing data under a simulated brain neural network architecture, enabling the chips to achieve high-speed parallel and low-power computing similar to the human brain. The combination of photonic chips based on micro-nano photonic integration and neural network data processing systems based on optical computing holds the key to addressing future information processing demands for low power consumption, high speed, wide bandwidth, and large data volumes.

6. Development Status of PECI in the Field of Intelligent Perception

With the continuous development of modern technologies such as 5G communications and artificial intelligence, perception systems based on PECI technology are facing more complex application scenarios, greater diversity in the heterogeneity of various systems, and increasingly rich information interaction methods. In this context, there is an urgent need for optoelectronic integrated perception systems to have intelligent and integrated capabilities to meet the application requirements of different scenarios, the interface types of different systems, and the data formats of different information.

In recent years, intelligent perception systems based on PECI have achieved some level of development. Depending on their position within the system, they can be divided into three parts: intelligent optoelectronic fusion front-end, intelligent optoelectronic fusion link, and intelligent optoelectronic fusion processing.

(1) Intelligent Optoelectronic Fusion Front-end for Signal Processing and Beamforming

The intelligent optoelectronic fusion front-end is designed to achieve broadband signal transceiving and beamforming. Its core components are the intelligent microwave photonic mixer and the true time delay (TTD) array. The fundamental principle of microwave photonic mixing is to convert radio frequency (RF) signals into the optical domain, forming optical carrier RF signals. These signals are then mixed with high-frequency, intelligently tunable optical local oscillators (LOs) to achieve high-quality mixing. In 2018, F. Scotti and his colleagues from the Italian National Laboratory for Photonics utilized a mode-locked laser to generate the optical LO, enabling tunable signal transceiving within the 2-18 GHz range.

The principle of beamforming based on the TTD array involves converting RF signals into the optical domain to form optical carrier RF signals. Different group delays are introduced to these signals using the optical TTD array. After optoelectronic conversion, a beam with a specific spatial orientation is formed. In this regard, in 2018, B. L. Anderson and his team from Ohio State University implemented an 81-channel TTD beamforming system based on optical frequency combs and integrated spatial optical devices.

Overall, the intelligent optoelectronic fusion front-end leverages the strengths of both optical and electronic technologies to achieve efficient and flexible signal processing and beamforming, critical for applications in modern communication and sensing systems.

(2) Intelligent Optoelectronic Fusion Link for High-Performance RF Signal Transmission

The intelligent optoelectronic fusion link facilitates high-performance transmission of radio frequency (RF) signals, incorporating technologies such as wavelength division multiplexing (WDM), routing and switching, and phase-stable transmission.

WDM technology is crucial for simultaneously transmitting multiple sets of

information. In 2019, P. T. Dat and colleagues from the National Institute of Information and Communications Technology in Japan achieved simultaneous transmission of millimeter-wave signals and LTE-A signals using WDM technology. When it comes to intelligent routing and switching of multiple information sets, optical switch arrays become necessary. In 2017, R. B. Priti et al. implemented an N×N optical switch array based on the Mach-Zehnder interferometer by controlling the phase difference between its two arms. In the same year, S. P. Wang et al. achieved path switching for different channels by adjusting the resonance wavelength of microring resonators through temperature control, enabling further expansion of the array size through cascading. During the transmission of optical carrier RF signals, non-ideal disturbances such as mechanical and temperature variations in the link can lead to significant phase jitter at the receiving end. Additionally, non-ideal factors like the nonlinear power transfer function of modulators can severely impact the dynamic range of microwave photonic links.

To address these challenges, in 2013, R. Zhu and his team from Concordia University in Canada achieved a spurious-free dynamic range (SFDR) of 110 dB·Hz2/3 using analog predistortion techniques. In 2014, W. Li and colleagues from the University of Ottawa, Canada, constructed an all-optical link linearization system based on a polarization modulator and a Sagnac loop, achieving an SFDR of 121 dB·Hz2/3 and third-order intermodulation distortion suppression greater than 50 dB. These advancements in intelligent optoelectronic fusion links demonstrate the potential for high-performance, reliable, and scalable RF signal transmission in modern communication systems.

(3) Intelligent Optoelectronic Fusion Processing for Broadband Signal Reception and Handling

Intelligent optoelectronic fusion processing facilitates the reception and handling of signals across a broadband spectrum. Two typical technologies in this domain are

optical channelization and photonic compressed sensing.

Optical channelization utilizes multiple parallel channels to receive RF signals within a broad frequency range. The core lies in the realization of the channelizer. Using flexible and tunable microwave photonic filters, reconfigurable channelizers can be achieved, enabling intelligent RF signal reception and processing. Additionally, for the RF signals received within each channel, they need to be converted into digital signals for further processing. Compressed sensing technology allows for the discrete sampling of signals at rates far below the Nyquist rate and subsequently reconstructs the original signal using algorithms. This technology is particularly useful in scenarios where signal bandwidth is extensive, but the sampling and processing capabilities are limited.

Moreover, regarding the integration of optoelectronic fusion-based intelligent sensing systems, the rapid development of silicon photonics has enabled high-performance devices and chips. For instance, in 2013, F. Horst and his colleagues used a cascaded Mach-Zehnder interferometer (MZI) structure with thermal tuning elements to realize a flat-response 1×8 wavelength division multiplexing (WDM) filter. They combined this with delay lines to construct a flat-top Nyquist-WDM filter, further optimizing the roll-off factor. In 2019, D. J. Liu et al. successfully developed a new MZI optical switch with a bandwidth of up to 140nm using bent directional couplers. This development paves the way for realizing large-scale N×N optical switch arrays and their applications. In 2017, D. Perez and his team proposed a hexagonal MZI-based optical processing chip capable of performing over 20 different functions, including ring resonators, single-input/single-output finite impulse response filters, and coupled-resonator optical waveguides.

Looking ahead, leveraging flexible and powerful artificial intelligence (AI) techniques combined with PECI technologies, intelligent sensing systems based on optoelectronic fusion integration are poised to achieve real-time interactions with the environment and users. These systems will play an increasingly critical role in intelligent scenarios, driving the next wave of technological advancements.

IV. Development Status in China

1. China's strategic layout in PECI

China's national key research and development program has launched special projects on "Optoelectronics and Microelectronics Devices and Integration" and "Information Photonics Technology," providing funding for photon integration in multi-material systems, photon integration chips with multi-dimensional control, and multi-functional integrated optoelectronic hybrid integrated computing systems. Currently, the development of PECI technology is still in its infancy, and key technological breakthroughs are needed in many aspects, including materials, simulation tools, core processes and foundry platforms, wafer-level characterization methods, and integration schemes.

2. Development status of process technology in China

In China, although there are no platforms similar to Intel or GlobalFoundries, with years of support from the national and local governments, a relatively complete manufacturing and processing platform and technological capability have been formed nationwide. From the perspective of operational models and technological capabilities, there are mainly three categories:

(1) University research experimental micro/nano processing platforms based on electron beam direct writing.

Such platforms are generally similar, with an investment scale of about 100-200 million yuan. They operate traditionally, have low standardization of process capabilities, and poor stability and repeatability of preparation processes. However, they are characterized by strong flexibility, which is conducive to exploring new materials, new processes, and new structures, and the device development cycle is relatively short. Relevant domestic units include: Semiconductor Institute, Zhejiang

University, Shanghai Jiaotong University, Huazhong University of Science and Technology, Northwestern Polytechnical University, Sun Yat-sen University, Westlake University, etc. Such platforms are generally geared towards passive devices and are usually equipped with core equipment such as electron beam lithography (with UV lithography), ICP dry etching, and PECVD thin film deposition. Among them, electron beam exposure equipment mainly comes in several specifications such as 30kV, 50kV, and 100kV, differing in characteristics such as electron beam direct writing speed and fineness. In principle, such platforms can be used for the preparation of photonic integrated devices in material systems such as silicon, SiN, and lithium niobate. Currently, most of them have the capability to prepare silicon optical waveguides and passive devices, and a few platforms have the capability to prepare SiN and lithium niobate optical waveguides (such as Sun Yat-sen University and Zhejiang University). Currently, there are significant differences in the process levels of various platforms. Taking the developed silicon optical waveguide as an example, its loss is usually 1-3 dB/cm, mainly determined by the lithography and etching processes involved in each platform. It is worth noting that the use of electron beam lithography eliminates the need for high-precision photomasks and allows for the preparation of fine structures in the range of 10-100 nm. However, it often has issues such as a small writing field (100-1000 micrometers), making it suitable for the preparation and principle verification of small-sized unit devices (especially silicon optical passive devices with sub-wavelength structures) and difficult to meet the development needs of large-scale integration.

(2) Commercial micro/nano processing platforms based on electron beam direct writing.

Such platforms have an investment scale of 200-500 million yuan, but the equipment types are similar to the first category, mainly including core equipment such as electron beam lithography (with UV lithography), ICP dry etching, and PECVD thin film deposition. However, they are equipped with a dedicated engineering team, have

stronger equipment specificity, more comprehensive coverage, better process stability, and better-performing electron beam direct writing equipment. Therefore, they have obvious advantages in processing capabilities compared to the first category and provide good support for developing new photonic devices with fine structures. Major representatives of such platforms include Tianjin Huahuixin, Nanjing Nanzhi Photoelectricity, Suzhou Nano Institute, etc., which can provide services for the preparation of photonic integrated devices in material systems such as silicon, SiN, and lithium niobate. The Nano Processing Platform of the Suzhou Institute of Nano-Tech and Nano-Bionics, Chinese Academy of Sciences, has a 10,000 m2 clean laboratory equipped with a complete set of process equipment for epitaxial growth, lithography, etching, chemical vapor deposition, physical vapor deposition, ion implantation, and device packaging. It has research and development capabilities for micro/nano electronic devices, micro-electromechanical systems, and optoelectronic devices. Its stepper lithography machine has a maximum resolution of 350 nm, and its electron beam lithography machine operates at 50 kV, but it does not directly provide standard manufacturing processes for silicon optical devices. As a provincial-level pilot platform supported by Tianjin Municipal Government, Huahuixin has a technical team of over 100 people, a 1,500 m2 clean laboratory, and a 18,000 m2 industrialization base. It is equipped with electron beam exposure machines (EBL), UV lithography machines, reactive ion etching equipment, and has micro/nano processing capabilities for various material systems such as SOI, thin-film lithium niobate (LNOI), and silicon nitride (SiN). However, it still lacks active silicon optical process capabilities such as ion implantation doping and germanium epitaxy. Its EBL equipment has a maximum voltage of 100 kV and a maximum writing field area of 1 mm × 1 mm. Representative processing capabilities include a minimum feature size of 60 nm for SOI optical waveguides and a single-mode waveguide transmission loss of 2 dB/cm. Compared to deep UV stepper lithography, its process steps can be flexibly customized, and the delivery cycle is shorter.

(3) Wafer-level foundry platforms based on DUV lithography.

Such platforms are similar to Belgium's IMEC, Singapore's AMF, etc. They have a complete set of silicon optical device manufacturing capabilities, including passive and active devices (such as modulation and detection), due to the availability of semiconductor doping, epitaxy, and other equipment. Representative domestic units include the Institute of Microelectronics of the Chinese Academy of Sciences, Chongqing CUMEC, and Shanghai Industrial Technology Research Institute. Currently, all three units can provide Si/SiN 8-inch wafer foundry services with 180nm processing capabilities, and CUMEC can provide 130nm processing services. The Shanghai Industrial Technology Research Institute offers two sets of silicon optical processes, including 90nm SOI active/passive processes and 180nm SiN passive processes. It has key process capabilities such as three-step silicon etching, multi-step active device doping, germanium epitaxy, TiN metal heating electrodes, dual-layer aluminum interconnects, and deep silicon etching, supporting the development of various silicon optical passive/active devices. Table 1 lists the representative metrics of these three platforms, showing significant differences in their processing capabilities. More importantly, there are differences in processing stability/repeatability among the platforms. A particular shortcoming is that the processing cycle is generally long or even too long. For example, active foundry may take up to a year to complete, and passive foundry often takes 4-6 months, making it difficult to meet the urgent needs of domestic PECI development. Therefore, there is an urgent need to continuously improve their processing capabilities.

Table 1. Performances of CUMEC、IMECAS and SITRI

	CUMEC	IMECAS	SITRI
Fabrication Lines	180nm-Si 180nm-SiN	180nm-Si 180nm-SiN	90nm-Si 180nm-SiN
SOI WG (Strip) Loss	1.5 dB/cm	2.5 dB/cm	2 dB/cm

SOI WG (Rib) Loss	1.0 dB/cm	1.5 dB/cm	/
SiN WG (Rib) Loss	<0.1dB/cm (Height 800 nm)	0.5dB/cm (Height 250nm)	0.15dB/cm (Height 400nm)
Dark Current of Ge-Si PD	<10nA @ -1V	100 nA @ -1V	<30nA @ -1V
Doping	B, P	B, P	B, P

In recent years, the thin-film lithium niobate (LNOI) platform has emerged as a prominent player in the field of photonics, with significant advancements in domestic manufacturing capabilities placing China at the forefront globally. Specifically, in terms of optical-grade thin-film lithium niobate wafers, Jinan Jingzheng and Shanghai Simgui are leading global enterprises in this space, offering a range of products with diverse film thicknesses (200-900nm) and substrate materials (quartz, silicon, sapphire), while ensuring stable supply.

Regarding the integration of thin-film lithium niobate into photonic chips, several institutions in China, including Zhejiang University, Sun Yat-sen University, Shandong University, East China Normal University, Shanghai Jiao Tong University, Tsinghua University, and City University of Hong Kong, have been at the forefront of related research. Each has developed unique processes on their respective fabrication platforms. Additionally, companies such as Guangzhou Neo-Optronic, Tianjin Huahuixin, and Nanjing Nanzhiguangdian also provide photonic chip foundry services for thin-film lithium niobate. The key aspects of fabricating these chips involve etching and pattern generation.

For etching, inductively coupled plasma (ICP) dry etching is commonly employed. This technique is used by various institutions and companies mentioned above due to its stability and efficiency. It achieves a waveguide transmission loss of 0.1dB/cm. However, due to the chemical stability of lithium niobate, sputter etching is often used in dry etching, resulting in waveguides with sidewall angles ranging from 60-70 degrees. Tianjin Huahuixin, for instance, fabricates LNOI waveguides with a minimum feature

size of 150nm, a single-mode waveguide transmission loss of 0.5dB/cm, and sidewall angles of 50°-60° (soft mask) or 70°-80° (hard mask). Recently, Tsinghua University developed a wet etching-based process for lithium niobate structures, achieving vertical sidewalls and a transmission loss of 0.04dB/cm, although this process may not be suitable for complex photonic chips. East China Normal University developed a chemical-mechanical planarization (CMP)-based etching process for lithium niobate, resulting in smooth sidewalls and a waveguide loss of 0.027dB/cm. However, the excessive sidewall angle limits chip integration.

In terms of pattern generation, electron beam lithography has been the earliest and most widely used technique both domestically and internationally. It stably produces structures with minimum dimensions of 100nm and is currently employed by various universities and research institutions in China, including Zhejiang University, Sun Yat-sen University, Tianjin Huahuixin, and Nanjing Nanzhiguangdian. Recently, institutions like City University of Hong Kong and Guangzhou Neo-Optronic have developed deep ultraviolet (DUV) lithography-based processes for lithium niobate chips, enabling 4-6 inch wafer-level fabrication with a minimum line width of around 220nm. This is suitable for high-volume production of traditional optical waveguide devices such as modulators and nonlinear devices.

3. Development Status of Systems and Applications in China

China has made significant progress in the field of PECI technology for communication applications in recent years, despite a later start compared to other countries. However, there is still a certain gap compared to international levels. Specifically, in short-distance optical interconnects, the National Information Optoelectronics Innovation Center has taken the lead in achieving large-scale industrial applications of 100G-400G series silicon photonic coherent and digital transceiver chips, breaking foreign monopolies. They have developed the world's first silicon-based lithium niobate thin-film coherent optical modulator and silicon-based graphene coherent optical receiver, launched the first 1.6Tb/s silicon photonic interconnect chip

and 1.4T silicon photonic coherent transceiver chip, and repeatedly set domestic and international records in silicon photonic modulator chips and detector chips.

In terms of inter-satellite and satellite-ground communications, the 504th Research Institute of China Aerospace Science and Technology Corporation achieved laser communication between the Shijian-20 satellite and ground with a maximum communication rate of 10Gbps and a communication distance of 40,000km in 2019. For air-ground-sea cross-domain communications, the 34th Research Institute of China Electronics Technology Group Corporation achieved balloon-ground laser communication in the stratosphere as part of the "Honghu" special mission in September 2021, with a communication rate of 2.5Gbps, a communication distance of 67km, and a payload weight of 23kg. In the field of underwater optical communications, institutions such as the Xi'an Institute of Optics and Precision Mechanics, Shanghai Institute of Optics and Fine Mechanics, and Wuhan Liubo Photoelectric have developed engineering prototypes and conducted applied research in areas such as deep-sea exploration and air-to-underwater cross-medium communication, achieving high-speed underwater information transmission over hundred-meter scales. For unmanned platform communications, the 34th Research Institute achieved laser communication between two multi-rotor unmanned aerial vehicles in June 2023, with a communication rate of 1.25Gbps, a communication distance of 30km, and a payload weight of 15kg.

In terms of optical computing, with the support of national and local government policies, China's optical computing industry has developed rapidly, initially forming an industrial chain that spans "design-manufacturing-prototyping." Significant attention and development have been given to design, processing, packaging, and testing technologies for optical computing chips, and there is a certain level of basic theory and practical experience in optical computing. China is keeping pace with Western developed countries in the field of optical computing and has reached a parallel level. Domestic universities, research institutions, and enterprises have mastered multiple autonomous control core technologies and developed various research products in the design, preparation, and testing of optical computing. However, optical computing

research and development in China is still in its infancy, facing challenges such as the inability to achieve joint simulation of optoelectronic and microelectronic chips, gaps in batch preparation processes and chip performance compared to international levels, and limitations in advanced packaging technologies. Nonetheless, significant progress has been made in areas such as high-performance photonic convolutional neural networks, photonic arithmetic acceleration chips, and waveguide-based optical computing, demonstrating China's growing capabilities and potential in this field.

Ⅴ. Development Suggestions

1. Overall Suggestions

In tackling the key scientific and technological issues in the field of PECI, the following overall task suggestions are proposed:

- Breaking the limitation of single material systems: Utilize existing materials such as silicon, III-V compounds, organic materials, and lithium niobate for PECI. Simultaneously, explore new materials and their mechanisms, tailored to the properties of different materials, to enhance the overall performance of integrated chips. For instance, employ heterogeneous integration to address the luminescence issues plaguing silicon-based material systems.
- Overcoming material dimensionality constraints: Pursue PECI across multiple material dimensions, ranging from 0D materials (quantum dots, nanocrystals) to 1D materials (quantum wires, carbon nanotubes), 2D materials (quantum wells, graphene), and 3D materials (silicon, photonic crystals). Approach the problem from multiple angles and dimensions to longitudinally demonstrate the regulation mechanism of PECI.
- Surpassing regulation dimensionality limits: Manipulate and harness physical parameters such as amplitude, polarization, frequency, time, phase, and space to maximize modulation bandwidth, chip transmission rates, and expand transmission capacity.
- Addressing chip manufacturing and packaging for PECI: Develop an PECI simulation platform that utilizes artificial intelligence to design microwave impedance matching with optical wave mode fields. This approach avoids signal reflection and loss during impedance and mode field transformations, enhancing efficiency. Automate the design of hybrid integration technologies such as wire bonding, ball welding, and Through-Silicon Vias (TSV).
- Efficient development and utilization of resources across various frequency

bands: Achieve spectral response in multiple bands, including microwave, millimeter wave, terahertz wave, infrared, visible, and ultraviolet. Scientific exploitation of these bands will bolster our country's spectrum resource reserves, alleviate pressure on spectrum capacity supply and demand, and provide abundant spectrum resources for the long-term development of PECI in China.

- Transcending functional limitations: Break through the constraint that chips can only perform a single function. Enhance the capabilities of monolithic optoelectronic integrated chips in information generation, acquisition, transmission, storage, display, amplification, processing, and complete multi-functional on-chip system integration.
- Integration of energy and information optoelectronics: Develop single-photon detection technology to achieve ultra-sensitive information sensing and processing capabilities. Target high-power, high-speed optical emission technology for ultra-long-distance information transmission spanning tens of thousands of kilometers.

2. Integrated Chip-Level Suggestions

(1) Silicon-Based Optoelectronic Integrated Chips

In the past few decades, research on silicon-based PECI technology has mainly focused on the 1.3μm and 1.55μm bands, relying on mature and high-precision silicon-based processing technology to achieve high-density wavelength division multiplexing in these bands. As the density of wavelength channels continues to increase, crosstalk between channels gradually increases, and the operating wavelength of silicon-based chips is gradually expanding towards the 2μm to 8.3μm band. This band also has lower absorption loss in silicon-based chips and has broad application prospects in fields such as gas sensing and biomedicine. Therefore, increasing investment in research and application of silicon-based optoelectronic integrated chip technology in the mid-

infrared band will be a focus of future work.

At the same time, emphasis should be placed on the development of silicon-based luminescent materials and devices that are compatible with CMOS processes, especially the research and development of new silicon-based light source materials. In addition, future research on silicon optoelectronic detection technology should focus on the following main aspects: firstly, improving dark current control and sensitivity of detectors; secondly, breaking through bandwidth limitations of detectors; and thirdly, enhancing detection efficiency and expanding wavelength range. By innovating key device processes and material structures, combining bandgap engineering with new materials, improving dark current characteristics, enhancing absorption efficiency of detectors in a wide spectral band, and comprehensively optimizing detector performance, once breakthroughs are achieved in the performance of silicon-based luminescent devices and detection devices, deep silicon-based PECI and large-scale mature commercialization of optoelectronic and microelectronic hybrid integrated chips will be realized.

(2) PECI Ultra-Large Scale Integrated Chips

In the long run, the goal is to achieve the integration of multiple functions such as light emission, transmission, amplification, detection, and processing, as well as the PECI of supporting drive and control circuits, using standard fabrication processes on the same integrated material system or the same wafer. The development of PECI requires the integration of various aspects across the entire chain of materials, design, processes, chips, packaging, and system applications.

(a) In terms of material systems, the heterogeneous integration of multiple materials is a fundamental issue that needs to be urgently addressed, with silicon-based light emission and amplification compensation being the top priorities.

(b) In terms of PECI design, it is necessary to gradually improve the basic theory of PECI and control, establish an integrated design environment for PECI, and

develop specialized tools for the entire design process including physical simulation, device modeling, link simulation, layout design, and verification, forming new design methodologies. Combined with domestic process platforms, it is necessary to develop an PECI component library for design automation and establish an independent and controllable integrated optoelectronic design ecosystem.

(c) In terms of process integration, it is necessary to fully utilize the mature CMOS platform, develop chip fabrication processes suitable for the integration of optoelectronics and microelectronics of different sizes, form technology solidification and standardization techniques and component libraries, and establish a stable and operational integrated process technology platform.

(d) In terms of PECI packaging, the bandwidth and throughput can be significantly improved and energy consumption reduced by integrating optical interfaces within high-performance integrated electrical packaging modules. It is necessary to develop optoelectronic packaging and testing technologies compatible with microelectronic testing processes, particularly wafer-level built-in self-test technologies and testing processes for large-scale manufacturing, and establish an optoelectronic integrated chip testing system and standards to address issues such as collaborative design of optoelectronic chips, packaging process integration, and power consumption and heat dissipation.

(e) In terms of PECI applications, it is necessary to promote multi-band, multi-dimensional, multi-material, and multi-functional PECI technologies, achieve the development of ultra-high-speed and ultra-low-power intelligent chips and modules, break through the bottlenecks of information transmission, sensing, and processing integration in optoelectronic technology, and achieve large-scale applications in fields such as ultra-high-capacity optical communication systems, 5G/B5G systems, high-performance optical computing, and

optoelectronic sensor networks.

(3) Microwave Photonic Chip

Integrated microwave photonic technology focuses on the research and development of core optoelectronic chips and integrated modules for the generation, transmission, processing, and reception of broadband microwave photonic signals. It provides implementation solutions for microwave photonic systems that are small in size, low in power consumption, array-based, and capable of rapid and intelligent reconfiguration. This technology is crucial for the full practical application and industrialization of microwave photonics and will become a core technology for applications such as the next-generation integrated space-air-ground information network, future broadband wireless access networks, radar, and electronic countermeasure systems.

(a) In terms of active core devices for microwave photonics, active devices such as lasers, modulators, and detectors are the core components of microwave photonic systems, determining the key performance indicators of the system. Currently, the bandwidth of domestically produced microwave photonic active devices is below 20GHz, while the international advanced level has reached up to 40GHz. Therefore, we should establish a processing platform targeted at advanced material systems and addressing the shortcomings of domestic processes, striving to achieve significant breakthroughs in the independent research and development of core optoelectronic devices.

(b) Regarding microwave photonic array devices, as the functionality of microwave photonic systems continues to increase, the number of unit devices required for system-on-chip integration also continues to grow. Achieving high-performance arraying of devices is a key technological breakthrough. Advanced array design and packaging can significantly improve system stability and sensitivity, increase linear range, and reduce size and power consumption noise, representing an important development direction for the

future.

(c) In terms of simulation design, packaging, and testing of microwave photonic chips, there is a need to develop new methods, models, and architectures, as well as to research and develop independent intellectual property rights for PECI simulation design software. Future research should focus on the theoretical research of optoelectronic co-simulation and the development of layout drawing software based on III-V and silicon-based materials, organizing domestic universities and research institutes to design high-performance device PDK libraries. In addition, it is necessary to establish and train chip simulation and layout design platforms to achieve intelligent full-chain simulation capabilities for optoelectronic design. Finally, the development of microwave photonic integrated chip packaging and testing platforms should encourage relevant research institutes and enterprises to research and develop advanced flip-chip bonding technology, multi-dimensional packaging technology, etc., to reduce packaging parasitic effects and break through the technical bottlenecks of analog high-frequency packaging and high-speed optoelectronic integrated packaging. Ultimately, the goal is to achieve a complete microwave photonic ecosystem, providing high-performance devices and modules for microwave photonic chip-level industrial applications in China.

(4) Photonic Intelligent Chip

In the field of photonic artificial neural networks, breakthroughs in PECI technology have enabled the research and development of large-scale arrayed optical computing chips with monolithic integration. This significantly enhances their integration density and computing speed. In some specific computing scenarios, large-scale optical networks can already perform calculations directly in the optical domain, achieving computing speeds that far exceed traditional microelectronic chips. The electrical control modules in these systems only adjust the network bias voltage,

realizing a truly all-optical intelligent neural network.

At this stage, the advantages of optical computing have been fully leveraged. The next step is to develop more application scenarios and vigorously promote the industrialization and practical use of photonic neural network chips. As PECI technology matures, the scale and computing speed of photonic neural networks will undergo significant enhancements. This will enable the development of more reconfigurable neural network functions, leading to the realization of a reconfigurable development platform for photonic neural networks. This platform will provide greater flexibility and adaptability for the further advancement of photonic artificial neural networks.

3. System and Application Suggestions

(1) Integrated Sensing and Computing Technology for High-Precision Multi-Dimensional Perception Imaging

Given the global diversity of static and dynamic targets and the complexity of environmental changes, to meet the national strategic demand for real-time global situational awareness, there is an urgent need for multi-spectral bands such as microwave, infrared, visible light, and terahertz, as well as multi-parameter multi-dimensional perception detection and fusion technologies such as intensity, phase, polarization, and spectrum. This results in a huge capacity for information transmission and processing, which is difficult to support with existing detection and communication processing technology solutions for realizing China's global real-time situational awareness capability. There is an urgent need to adopt PECI technology combined with multi-sensor fusion detection imaging, multi-dimensional signal processing, intelligent control information processing, and target recognition. Research on PECI technology that integrates sensing, storage, and computing is needed to break through key technologies such as the integrated mechanism of "optical sensing, magnetic storage, and electronic computing," information processing algorithms, integrated circuits and

architectures, and heterogeneous integration processes. This will significantly enhance the capability of precise perception and relieve the pressure on backbone communication links and central processing, enabling wide applications in networked platforms such as drone swarms, unmanned combat vehicles, small satellite constellations, and underwater unmanned vehicles. This provides core technological support for achieving global reconnaissance strategic goals.

(2) Never-Dropping Spatial Laser Backbone Communication Networking Technology

Currently, most laser communication systems use mechanical rotation to achieve "point-to-point" single-target motion area coverage. Laser communication suffers from issues such as easy link dropping and difficulty in alignment, making it challenging to effectively support rapid access and networking applications among multiple terminals. The communication rate is low, and the survivability is weak. Ultra-high-speed multi-target spatial laser communication systems based on optical phased array technology adopt key technologies such as optical phased array multi-access, high-power spatial laser transmission, multi-carrier multiplexing, ultra-high-speed adaptive spatial laser demodulation, and silicon-based integrated coherent reception. This enables spatial scanning of one or multiple high-intensity laser beams, significantly improving networking, performance, and quality. It forms multiple stable spatial laser backbone links with high throughput and efficient coordination, meeting the communication needs of cross-domain and even full-domain operations. This provides core technological support for efficient networking of large-scale satellite constellations, enabling autonomous decision-making and multi-dimensional approaches for enemy strikes.

(3) Ultra-Large Capacity and Ultra-Low Power Optical Communication Chips and Modules

PECI is expected to combine the advantages of optoelectronics and microelectronics in ultra-high frequency and high efficiency, breaking through existing bottlenecks in speed and energy consumption. By achieving breakthroughs in the design, preparation, packaging, and measurement of ultra-large bandwidth optoelectronic modulation and detection devices, autonomous control of core optical communication devices with bandwidths exceeding 200 GHz can be achieved. By studying the design, preparation, packaging, and measurement of ultra-high-frequency high-power efficient electric drive and amplification chips, the integration of microelectronic chips and high-speed optical communication devices can be achieved. Through systematic research on carrier transport mechanisms and behavior under ultra-high frequency, ultra-strong field, and nanoscale conditions, new principles and high-performance PECI devices can be explored.

(4) Multi-Chiplet Optical Computing/Sensing System

Multi-functional PECI systems for intelligent sensing and computing are expected to achieve breakthroughs in scale, computing power, energy efficiency, and functionality. Developing heterogeneous packaging and integration technologies based on different functional chiplets can achieve high-performance computing and sensing systems that break through the limitations of a single chip's manufacturing process, yield, complexity, size, and cost. This can drive their applications in areas such as artificial intelligence inference, autonomous driving, and the Internet of Things.

(5) Co-Packaged Integration and High-Speed Inter-Chip Connectivity

As internal traffic in data centers continues to grow rapidly, switch capacity, port density, and interface speed face significant challenges. The PECI co-packaging solution, which directly packages the optical transceiver module and the electrical switching chip on the same substrate into a single chip, eliminates many SerDes functions and is expected to reduce energy consumption by 30%-80%. By achieving breakthroughs in high-speed optoelectronic modulation detection devices, developing

800G+ optical engine chips, and studying their co-packaging integration with switching chips, it is expected to achieve the next generation of high-performance and low-power switches for data centers. Additionally, optical I/O technology enabled by PECI chips can achieve efficient optical interconnectivity between chips, providing significant improvements in ultra-high bandwidth density, ultra-low latency, and system energy efficiency. By achieving breakthroughs in the core processes of optical I/O chips and developing new packaging processes with chips such as CPUs/GPUs/HBMs, efficient interconnectivity between computing, storage, and other chips can be achieved, enabling the construction of high-performance computing systems.

(6) Process Platform Technology for PECI

Currently, there are no unified specifications and standards for different optoelectronic devices. Traditional photonic, radio frequency, and microelectronic chips often have size differences of 1-2 orders of magnitude. To achieve optimal performance, various components adopt different structures and material systems. Currently, most photonic links, radio frequency circuits, and control drive circuits are designed separately and independently placed, resulting in high complexity and difficulty in integrating optoelectronic system architectures that combine the broadband high-speed characteristics of photonic technology with the fine and flexible advantages of electronic technology. This makes it challenging to reduce volume, weight, and power consumption. Most systems are based on discrete device verification, resulting in poor system functionality scalability. This cannot meet the demands for miniaturization, low power consumption, and high reliability. Therefore, it is necessary to study the physical basis of microelectronics-optoelectronics integration processes, address system-level control technology bottlenecks caused by structural differences across wavelengths, materials, and scales, and explore new principles and technologies for PECI. This will enable the realization of a new architecture for PECI with integrated and coordinated capabilities.

VI. Funding Mechanisms and Policy Recommendations

1. It is recommended to initiate the "Major Research Plan for Photonics-Electronics Convergence and Integration" under the National Natural Science Foundation of China to strengthen systematic research on PECI.

Driven by this major research plan, a comprehensive theoretical framework for PECI should be established, spanning from devices to chips and systems. This would involve breaking through a series of collaborative simulation and design techniques for optical and electrical circuits, and promoting standardized, intelligent, and automated simulation and design tools. Focusing on application needs such as optical communication/interconnection, optical computing, optical sensing, and optical measurement, research should prioritize ultra-high-speed optical transceiver and multiplexing technologies, intelligent optical signal recognition, and automated regulation and uniformity techniques. Efforts should also be made to layout CMOS-compatible processes geared towards large-scale and mass-producible pathways.

2. Increase investment in research and development (R&D) for PECI processes and enhance the upstream and downstream industrial ecosystem.

The challenge in the development of optoelectronic integrated circuits lies in the limitations of equipment and process conditions. Fabricating optoelectronic integrated chips requires new manufacturing techniques, which domestic companies are currently unable to achieve for fully integrated optoelectronic chips. It is recommended to increase central government funding, accelerate fundamental and technological innovation, collaborate with domestic optoelectronic and microelectronic institutions, coordinate upstream and downstream industries, deploy major projects in phased

manners, and tackle core process technologies for PECI.

3. Establish a standardized system for PECI design and fabrication techniques to unite efforts in integrated and collaborative PECI technology.

Currently, there is a lack of unified specifications and standards for various optoelectronic devices. Traditional photonic, radio frequency, and microelectronic chips often exhibit size differences of 1-2 orders of magnitude, and various components employ different structures and materials to optimize performance. It is recommended to deeply coordinate and customize the optical and electrical circuits in PECI, establish a public platform for processing optoelectronic integrated chips, provide technical support and services for the R&D and production of new PECI processes, integrate scattered R&D efforts in the industry, improve the innovation system and industrial ecosystem, and enhance the international voice of the industry as a whole.